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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

YOSHITAKA TERAO *et al.*

Serial No.:	10/045,017	Examiner:	MACCHIAROLO, PETER J.
Filed:	15 January 2002	Art Unit:	2875

For: PLASMA DISPLAY PANEL HAVING SPECIFIC RIB CONFIGURATION (as amended)

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97 and 1.98 as amended, Applicant cites, describes, and provides copies of the following art references:

U.S. PATENT REFERENCES:

- U.S. Patent No. RE37,444 to Kanazawa, entitled *METHOD AND APPARATUS FOR DRIVING DISPLAY PANEL*, reissued on 13 November 2001;
- U.S. Patent No. 5,541,618 to Shinoda, entitled *METHOD AND A CIRCUIT FOR GRADATIONALLY DRIVING A FLAT DISPLAY DEVICE*, issued on 30 July 1996;
- U.S. Patent No. 5,661,500 to Shinoda *et al.*, entitled *FULL COLOR SURFACE DISCHARGE TYPE PLASMA DISPLAY DEVICE*, issued on 26 August 1997;
- U.S. Patent No. 5,663,741 to Kanazawa, entitled *CONTROLLER OF PLASMA DISPLAY PANEL AND METHOD OF CONTROLLING THE SAME*, issued on 2 September 1997;
- U.S. Patent No. 5,674,553 to Sinoda *et al.*, entitled *FULL COLOR SURFACE DISCHARGE TYPE PLASMA DISPLAY DEVICE*, issued on 7 October 1997;

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- U.S. Patent No. 5,724,054 to Shinoda, entitled *METHOD AND A CIRCUIT FOR GRADATIONALLY DRIVING A FLAT DISPLAY DEVICE*, issued on 3 March 1998;

- U.S. Patent No. 5,786,794 to Kishi *et al.*, entitled *DRIVER FOR FLAT DISPLAY PANEL*, issued on 28 July 1998;

- U.S. Patent No. 5,952,782 to Nanto *et al.*, entitled *SURFACE DISCHARGE PLASMA DISPLAY INCLUDING LIGHT SHIELDING FILM BETWEEN ADJACENT ELECTRODE PAIRS*, issued on 14 September 1999;

- U.S. Patent No. 6,630,916 to Shinoda, entitled *METHOD AND A CIRCUIT FOR GRADATIONALLY DRIVING A FLAT DISPLAY DEVICE*, issued on 7 October 2003; and

- U.S. Patent No. 6,707,436 to Setoguchi *et al.*, entitled *METHOD FOR DRIVING PLASMA DISPLAY PANEL*, issued on 16 March 2004.

FOREIGN PATENT REFERENCES:

- Japanese Patent Publication No. 01-043804 to Komatsu *et al.*, entitled *PLASMA DISPLAY AND MANUFACTURE THEREOF*, published 16 February 2001.

- Japanese Patent No. 2917279 issued on 23 April 1999, and the related Patent No. 2845183 issued on 30 October 1998, and Publication No. 02-148645 published on 7 June 1990, to Nanto *et al.*, entitled *GAS DISCHARGE PANEL*, together with an English language Abstract and translation of the specification.

OTHER DOCUMENTS:

- "*Final Draft International Standard*", Project No. 47C/61988-1/Ed.1; Plasma Display Panels - Part 1: Terminology and letter symbols, published by International Electrotechnical Commission, IEC. in 2003, and Appendix A - Description of Technology, Annex B - Relationship Between Voltage Terms And Discharge Characteristics; Annex C - Gaps and Annex D - Manufacturing.

DISCUSSION

Kanazawa U.S '444 relates to an apparatus and method for driving a display panel, e.g., an AC PDP, having a first substrate, at least one display line including first electrodes and second electrodes disposed in parallel with each other on the first substrate, a second substrate facing the first substrate, and third electrodes disposed on the second substrate and extending orthogonally to the first and second electrodes, in which write operations of the display data by light emission is executed by carrying out a selective write discharge utilizing a memory function, which as adapted to execute a write discharge for all cells and to execute an erase discharge for all cells before the selective write discharge, to thereby accumulate wall charges over the third electrodes in advance. .

Shinoda U.S.'618 relates to a method and circuit of driving a flat display panel formed of a plurality of cells each having a memory function, where the cells are formed at cross points of a plurality of X-electrodes and a plurality of Y-electrode orthogonal to the X-electrodes, a period of a frame for displaying a single picture is divided into a plurality of sequential subframes. Each of the subframes has an addressing period during which cells to be lit later in a display period are selected from all the cells by being written by having a wall charge therein; and the display period subsequent to the address period for lighting the selected cells by applying sustain pulses to all the cells. A number of the sustain pulses included in each display period is predetermined differently for each subframe according to the weight given to each subframe. Gradation of visual brightness of each cell is determined by the accumulated number of the sustain pulses included in the subframes that are selectively operated during a single frame according to a required brightness level for each cell. Thus, an adequate time length is asserted to be allocated to required numbers of subframes to achieve a quality brightness-gradation for each cell.

Shinoda *et al.*U.S.'500 relates to a full color three electrode surface discharge type plasma display device that has fine image elements and is large and has a bright display. The three primary color luminescent areas are arranged in the extending direction of the display electrode pairs in a successive manner and an image element is composed by the three unit luminescent areas defined

by these three luminescent areas and address electrodes intersecting these three luminescent areas. Further, phosphors are coated not only on a substrate but also on the side walls of the barriers and on address electrodes. The manufacturing processes and operation methods of the these constructions are also disclosed.

Kanazawa U.S.'741 relates to a controller for a plasma display having a first drive unit to apply voltage to a sustain electrode of a display unit having a memory function and a second drive unit to apply voltage to an address electrode of the display unit. The first drive unit has a discharge control unit to control the discharge waveform of the voltage applied to the sustain electrode of the display unit. The discharge control unit has a delay element and a switching element connected in series between sustain electrodes. Alternatively, the control unit has a delay element and a switching element connected in series between the sustain electrodes and a constant voltage discrimination element connected in parallel with the delay element.

Shinoda *et al.*U.S.'553 relates to a full color three electrode surface discharge type plasma display device that has fine image elements and is large and has a bright display. The three primary color luminescent areas are arranged in the extending direction of the display electrode pairs in a successive manner and an image element is composed by the three unit luminescent areas defined by these three luminescent areas and address electrodes intersecting these three luminescent areas. Phosphors are coated not only on a substrate but also on the side walls of the barriers and on address electrodes. The manufacturing processes and operation methods of these constructions are also disclosed.

Shinoda U.S. '054 relates to a method and circuit for driving a flat display panel formed of a plurality of cells each having a memory function, where the cells are formed at cross points of a plurality of X-electrodes and a plurality of Y-electrode orthogonal to the X-electrodes, a period of a frame for displaying a single picture is divided into a plurality of sequential subframes. Each of the subframes has an addressing period during which cells to be lit later in a display period are selected

from all the cells by being written by having a wall charge therein; and the display period subsequent to the address period for lighting the selected cells by applying sustain pulses to all the cells. A number of the sustain pulses included in each display period is predetermined differently for each subframe according to the weight given to each subframe. Gradation of visual brightness of each cell is determined by the accumulated number of the sustain pulses included in the subframes that are selectively operated during a single frame according to a required brightness level for each cell. Thus, an adequate time length can be allocated to required numbers of subframes to achieve a quality brightness-gradation for each cell.

Kishi U.S.'794 relates to a flat panel display that has a low withstand voltage and performs high speed line sequential scanning and recovers power. An AC type panel display has electrodes arranged in a matrix form, a push-pull type driver circuit, having first and second transistors, provided for each pair of plural pairs, with power supply lines connected to a driver circuit for driving a plurality of display electrodes to be scanned and a power supply which supplies a defined voltage to one of the respective power supply lines of each pair connected to the corresponding driver circuit, and a leakage control switch which leaks the defined voltage applied to the power supply line.

Nanto *et al.*U.S.'782 relates to a surface discharge type plasma display panel(PDP) which includes a pair of front and rear substrates (11, 21) with a discharge space (30) therebetween and a plurality of pairs of display electrodes on an internal surface of either the front or rear substrate. The display electrodes extend along each display line L. The PDP further includes a light shielding film (45), having a belt shape extending along the display line direction, formed on either internal or outer surface of the front substrate (11) to overlap each area S2 between the adjacent display lines L and is sandwiched between the display electrodes X and Y.

Shinoda U.S. '916 relates to a method and circuit of driving a flat display panel formed of a plurality of cells each having a memory function, wherein the cells are formed at cross points of

a plurality of X-electrodes and a plurality of Y-electrodes orthogonal to the X-electrodes, and a period of a frame for displaying a single picture is divided into a plurality of sequential subframes. Each of the subframes has an address period, during which cells to be lit later in a display period are selected from among all of the cells by being written so as to have a wall charge therein, and a display period, subsequent to the address period, for lighting the selected cells by applying sustain pulses to all the cells. A number of sustain pulses included in each display period is predetermined differently for each subframe, according to a weight given to each subframe. Gradation of visual brightness of each cell is determined by the accumulated number of the sustain pulses included in the subframes that are selectively operated during a single frame according to a required brightness level for each cell. An adequate time accumulation is thereby allocated to a required number of subframes to achieve a quality brightness-gradation for each cell.

Setoguchi *et al.*U.S.'436 discloses a method for driving a plasma display panel in which a plurality of first electrodes and second electrodes are arranged parallel to each other, a plurality of third electrodes are arranged to cross the first and second electrodes, and discharge cells are defined with areas in which the electrodes cross mutually are arranged in the form of a matrix. According to the driving method, a reset period is a period during which the distribution of wall charges in the plurality of discharge cells is uniformed. An addressing period is a period during which wall charges are produced in the discharge cells according to display data. A sustain discharge period is a period during which a sustained discharge is induced in the discharge cells in which wall charges are produced during the addressing period. The driving method in accordance with the present invention has a step of applying a first pulse in which an applied voltage varies with time so as to induce a first discharge in the lines defined by the first and second electrodes, and a step of applying a second pulse in which an applied voltage varies with time so as to induce a second discharge as erase an discharge in the lines defined by the first and second electrodes. These steps are carried out during the reset period.

Komatsu *et al.* JP' 804 relates to a pattern 12P which is formed by photoresist 12R on substrate glass 12A, and substrate glass 12A in a part the pattern 12P is cut by sandblast to form a partition wall 18. After a process for cutting the substrate glass 12A and forming the partition wall 18, a process for forming an electrode 16 on the substrate glass 12 and a process for forming a phosphor 19 within a discharge cell 17 are performed and the partition wall 18 is constituted integrally with the substrate glass 12.

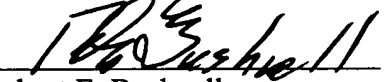
Nanto *et al.*, JP' 279, JP' 645, and JP' 183 (which is a divisional of Nanto *et al.* '279), together with an English language Abstract and translation of the specification, all relate to an electrode support base 11 which is formed of a transparent glass base, and mutually adjacent discharge keeping electrodes of each pair of transparent discharge keeping electrodes on the base, for example, between 321 and 312, are short circuited by a thick metal material layer 33 such as gold Au. When a voltage pulse is applied to the electrode drawing metal material layer 33, the discharge also simultaneously occurs in a read discharge cell related to the adjacent non-selected keeping discharge cell to which the voltage pulse is applied. By the discharge of the selected keeping discharge cell, a phosphor 23 provided on a cover base 21 generates an excited color display light and directly exhibits a color display on the display observing surface of the transparent electrode support base 11, to permit an observer to visually recognize a highly bright and clear color display.

The "***Final Draft International Standard***", Project No. 47C/61988-1/Ed.1, presents a list of nomenclature and a corresponding explanation of the nomenclature, together with waveform components, and Appendix A - Description of Technology; Annex B - Relationship Between Voltage Terms And Discharge Characteristics; Annex C - Gaps and Annex D - Manufacturing; collectively describe and graphically illustrate the principles of operation and manufacture for plasma display panels (PDP's) contemporary to the industry.

The citation of the foregoing references is not intended to constitute an assertion that other or more relevant art does not exist. Accordingly, the Examiner is requested to make a wide-ranging and thorough search of the relevant art.

A fee of $180.00 is incurred by filing this Information Disclosure Statement. Applicant's check drawn to the order of Commissioner accompanies this Information Disclosure Statement. Should there be any deficiency in payment, or should other fees be incurred, the Commissioner is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,



Robert E. Bushnell
Reg. No.: 27,774

1522 "K" Street, N.W., Suite 300
Washington, D.C. 20005
Area Code: (202) 408-9040

Folio: P56664
Date: 4 June 2004
I.D.: REB/gc/sb

INFORMATION DISCLOSURE STATEMENT PTO-1449 (PAGE 1 OF 1)	SERIAL NUMBER 10/045,017	DOCKET NO. P56664
	APPLICANT YOSHITAKA TERAO *et al.*	
	FILING DATE 15 January 2002	GROUP 2875

JUN 04 2004 PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	RE37,444	11/01	*Kanazawa*			
	5,541,618	07/96	*Shinoda*			
	5,661,500	08/97	*Shinoda et al.*			
	5,663,741	09/97	*Kanazawa*			
	5,674,553	10/97	*Sinoda et al.*			
	5,724,054	03/98	*Shinoda*			
	5,786,794	07/98	*Kishi et al.*			
	5,952,782	09/99	*Nanto*			
	6,630,916	10/03	*Shinoda*			
	6,707,436	03/04	*Setoguchi et al.*			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLAS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	JP 2001-043804 ✓	02/01	JAPAN			Abstract	
	JP 2917279 ✓	04/99	JAPAN			Abstract	
	JP 02-148645 ✓	06/90					
	JP 2845183 ✓	10/98					

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	"*Final Draft International Standard*", Project No. 47C/61988-1/Ed.1; Plasma Display Panels - Part 1: Terminology and letter symbols, published by International Electrotechnical Commission, IEC. in 2003, and Appendix A - Description of Technology, Annex B - Relationship Between Voltage Terms And Discharge Characteristics; Annex C - Gaps and Annex D - Manufacturing ✓

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

PTO/SB/17 (08-00)
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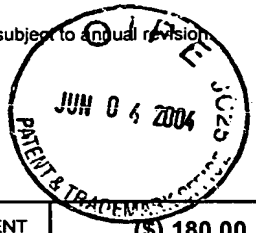
FEE TRANSMITTAL

Patent fees are subject to annual revision.



TOTAL AMOUNT OF PAYMENT	($) 180.00

Complete If Known	
Application Number	10/045,017
Filing Date	15 January 2002
First Named Inventor	YOSHITAKA TERAO et al.
Examiner Name	MACCHIAROLO, PETER J.
Group/Art Unit	2875
Attorney Docket No.	P56664

METHOD OF PAYMENT (check one)

1. ■ The Commissioner is hereby authorized to charge ANY DEFICIENCY to:

Deposit Account Number: 02-4943
Deposit Account Number: _____

☐ Charge Any Additional Fee Required Under 37 C.F.R. §1.16 and 1.17.

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ■ **Payment Enclosed: (CHECK #45680)**

■ Check ☐ Credit Card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	$
1002	340	2002	170	Design filing fee	$
1003	530	2003	265	Plant filing fee	$
1004	770	2004	385	Reissue filing fee	$
1005	160	2005	80	Provisional filing fee	$

SUBTOTAL (1) ($) .00

2. EXTRA CLAIM FEES

		Extra Claims	Fee from below	Fee Paid
Total claims	-20** =		x	=
Independent Claims	- 8** =		x	=
Multiple Dependent				=

** *or number previously paid, if greater; For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1201	86	2201	43	**Independent claims in excess of 3**
1202	18	2202	9	**Claims in excess of 20**
1203	290	2203	145	**Multiple dependent claim, if not paid**
1204	86	2204	43	**** Reissue independent claims over original patent**
1205	18	2205	9	**** Reissue claims in excess of 20 and over original patent**

SUBTOTAL (2) ($) .00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge-late filing fee or oath	$
1052	50	2052	25	Surcharge-late provisional filing fee or cover sheet	$
1053	130	1053	130	Non-English specification	$
1812	2,520	1812	2,520	For filing a request for reexamination	$
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	$
1805	1,840 *	1805	1,840*	Requesting publication of SIR after Examiner action	$
1251	110	2251	55	Extension for reply within first month	$
1252	420	2252	210	Extension for reply within second month	$
1253	950	2253	475	Extension for reply within third month	$
1254	1,480	2254	740	Extension for reply within fourth month	$
1255	2,010	2255	1,005	Extension for reply within fifth month	$
1401	330	2401	165	Notice of Appeal	$
1402	330	2402	165	Filing a brief in support of an appeal	$
1403	290	2403	145	Request for oral hearing	$
1451	1,510	1451	1,510	Petition to institute a public use proceeding	$
1452	110	2452	55	Petition to revive - unavoidable	$
1453	1,330	2453	665	Petition to revive - unintentional	$
1501	1,330	2501	665	Utility issue fee (or reissue)	$
1502	480	2502	240	Design issue fee	$
1503	640	2503	320	Plant issue fee	$
1460	130	1460	130	Petitions to the Commissioner	$
1807	50	1807	50	Processing fee for provisional applications	$
1806	180	1806	180	Submission of Information Disclosure Statement	$180.00
8021	40	8021	40	Recording each patent assignment per property (Times number of properties)	$
1809	770	2809	385	Filing a submission after final rejection (37 C.F.R. §1.129(a))	$
1810	770	2810	385	For each additional invention to be examined (37 C.F.R. §1.129(b))	$
1801	770	2801	385	Request for Continued Examination (RCE)	$
Other Fee (specify) _____					$
Other Fee (specify) _____					$

** Reduced by Basic Filing Fee Paid

SUBTOTAL (3) $ 180.00

SUBMITTED BY

Typed or Printed Name	Robert E. Bushnell, Esq.	Reg. Number	27,774
Signature	/Robert E. Bushnell/	Date	4 June 2004
		Deposit Account User ID	

REB/sb

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